User manual TUeDACS/3
IEEE-488 interface

BLN 2000-17 UM

May 2001

Eindhoven University of Technology
Department of Physics

Technical Laboratory Automation Group

Authors: R. Smeets
Version: 1.0
Date: 30-05-2001

Hardware design: G. A. Harkema

General guidelines for programming TUeDACS interfaces

1. After a TUeDACS interface is started or enabled, by setting the start bit (STR bit), enable bit (ENA bit) or the combined start/enable bit (STR/ENA bit) in the TUeDACS Status Word Register at interface subaddress 0x00, do *not* change any interface settings by changing the contents of write-only or read/write registers, as this may result in erroneous interface operation. Settings can be safely changed *before* starting or enabling the interface, i.e. when the DONE-bit in the TUeDACS Status Word Register at subaddress 0x00 is set.

2. If a specific TUeDACS interface must be programmed to use interrupts, follow these guidelines:

   - ❑ if the TUeDACS interface has a start bit (STR bit) in the TUeDACS Status Word Register at interface subaddress 0x00, the STR bit and the IE bit *must* be set at the same time.

   - ❑ if the TUeDACS interface has an enable bit (ENA bit) in the TUeDACS Status Word Register at interface subaddress 0x00, *first* set the ENA bit in the TUeDACS Status Word Register, *then* set the Interrupt Enable bit (IE bit) in the TUeDACS Status Word Register. Do *not* set the ENA bit and the IE bit at the same time, as this will result in a TUeDACS interrupt that is not caused by an ‘interface operation completed’ event.

   - ❑ if the TUeDACS interface has a combination of a start bit and an enable bit (STR/ENA bit) in the TUeDACS Status Word Register at interface subaddress 0x00, the function of the STR/ENA bit (start interface or enable interface) depends on a software-selectable interface-specific operating mode. In this case, the STR/ENA bit and the IE bit *must* be set at the same time (this does *not* depend on the selected operating mode, i.e. whether the STR/ENA bit is used as a start bit or as an enable bit).

3. Do not remove or insert a TUeDACS interface if the TUeDACS system crate is powered, as this may result in damage to TUeDACS interfaces and/or to the system crate.

1. Introduction 5

2. Block diagram 7

3. Programming model of the IEEE-488 interface 9
3.1 TUeDACS Status Word Register 10
3.2 Bus Address Switch Register 11
3.3 Interrupt Select Register 12
3.4 Interface Identification Register 12
3.5 Interrupt Status Register 0 / Interrupt Status Register 1 13
3.6 Interrupt Mask Register 0 and 1 14
3.7 Address Status Register 15
3.8 Auxiliary Command Register 16
3.8.1 Description of Auxiliary Commands 19
3.9 Address Register 24
3.10 Bus Status Register 25
3.11 Serial Poll Register 26
3.12 Command Pass Through Register 27
3.13 Parallel Poll Register 27
3.14 Data In Register 28
3.15 Data Out Register 29

4. DIP switch settings 31

5. LED indicators 33

1. Introduction

The TUeDACS/3 IEEE-488 interface (BLN 2000-17) interfaces IEEE-488 compatible devices and equipment to the TUeDACS system.

The TUeDACS/3 IEEE-488 interface is generally used as a controller on the IEEE-488 bus. The IEEE-488 interface specifications meet the IEEE-488 1975/1978 standard and 1980 supplement. All IEEE-488 equipment can be controlled by the TUeDACS system using this TUeDACS interface. IEEE-488 equipment is connected with the IEEE-488 interface using a standard IEEE-488 cable.

The TUeDACS/3 IEEE-488 interface is based on the industry standard 9914 IEEE-488 bus controller chip.

2. Block diagram

The block diagram of the TUeDACS/3 IEEE-488 interface is given in figure 2.1.

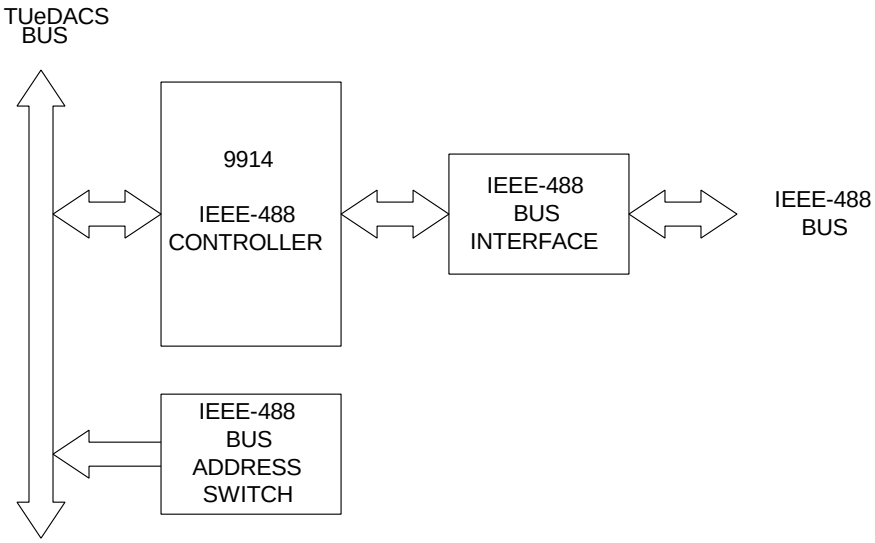

Figure 2.1 Block diagram TUeDACS/3 IEEE-488 interface

3. Programming model of the IEEE-488 interface

The programming model of the TUeDACS/3 IEEE-488 interface is given in figure 3.1.

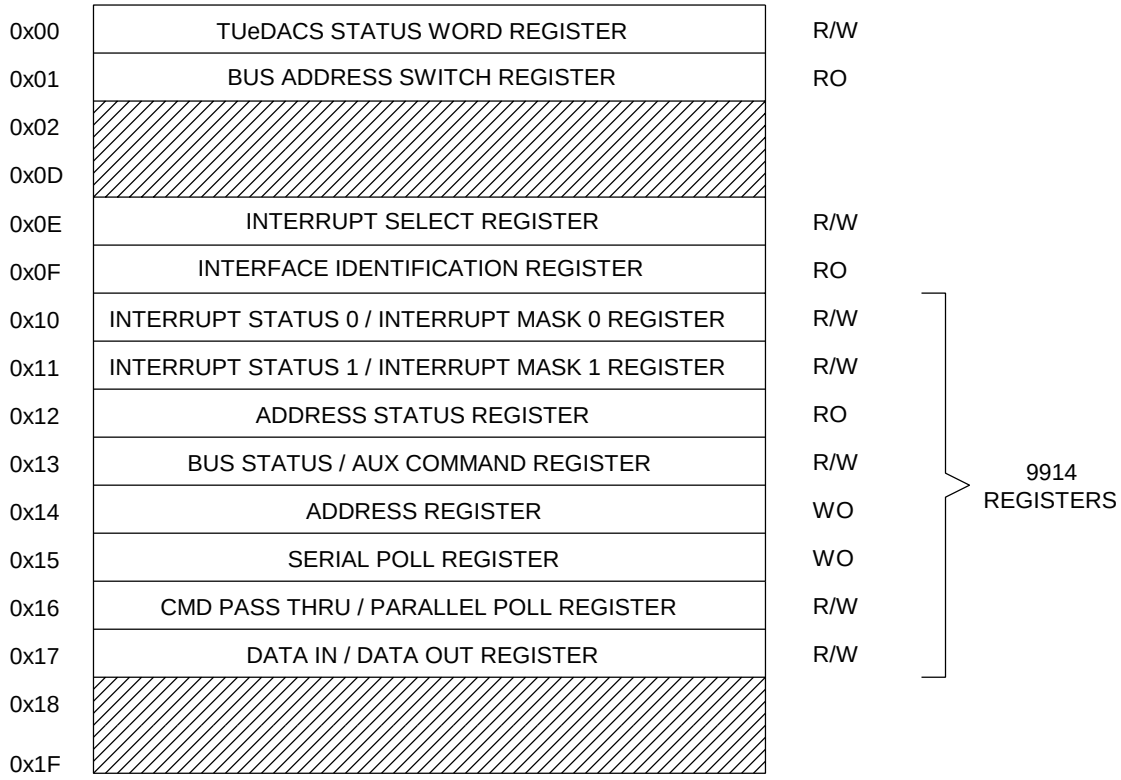

Figure 3.1 TUeDACS/3 IEEE-488 interface programming model

In this programming model, the 9914 chip (located at subaddresses 0x10..0x17) may have *two* registers located at *one* subaddress: one read register and one write register. If two such registers are located on a 9914 subaddress, the programming model shows the name of the read register first, and the name of the write register second.

3.1 TUeDACS Status Word Register

This 16-bit read/write register at subaddress 0x00 contains the standard TUeDACS status bits.

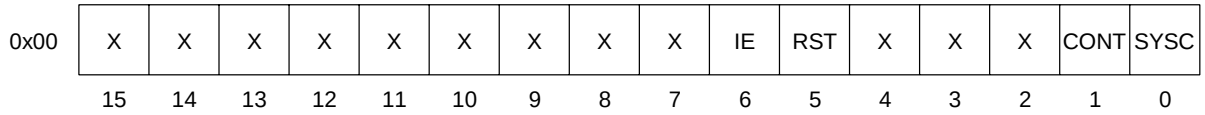

Figure 3.2 TUeDACS Status Word Register

bit	mnemonic	R/W	description
15..7	-	-	not used, reads as zero
6	IE	R/W	Interrupt Enable
5	RST	WO	ReSeT
4..2	-	-	not used, reads as zero
1	CONT	RO	CONTroller
0	SYSC	R/W	SYStem Controller

IE (bit 6): Interrupt Enable. If this bit is set, a TUeDACS interrupt is generated if one or more specified events occurs on the IEEE-488 bus. The events allowed to generate an interrupt, are selected with Interrupt Mask Register 0 at subaddress 0x10 and Interrupt Mask Register 1 at subaddress 0x11 (see section 3.6). If the IE bit is cleared, no TUeDACS interrupt can be generated by an IEEE-488 event.
The IE bit is cleared when issuing a software TUeDACS bus initialisation command.

RST (bit 5): setting this bit performs a hardware reset of the 9914 controller chip. Setting the RST bit does not change the contents of any other registers. Setting the RST bit is a one-time command. This bit need not be cleared.

CONT (bit 1): the read-only CONT (CONTroller) bit is set by the 9914 when the IEEE-488 interface is an active IEEE-488 controller. An active IEEE-488 controller may assert the ATN line and monitors the SRQ line.

SYSC (bit 0): the SYSC (SYStem Controller) bit must be set during normal operation, i.e. when the IEEE-488 interface is a system controller. The direction of the IEEE-488 bus lines IFC and REN is controlled by this bit. If the SYSC bit is set, the IFC and REN lines are wired as outputs. After a power-up or, or if a TUeDACS bus initialisation command has been issued, the SYSC bit must be set.

3.2 Bus Address Switch Register

This 16-bit read-only register at subaddress 0x01 is used to read the DIP switch value containing the IEEE-488 bus address. The IEEE-488 bus address of the interface can be selected using an 8-position DIP switch, of which only switch positions 1..5 are used (positions 6..8 are unused). The selected address can be read by software. To use this IEEE-488 bus address, the contents of the Bus Address Switch Register must be written to the Address Register of the 9914 at subaddress 0x14.

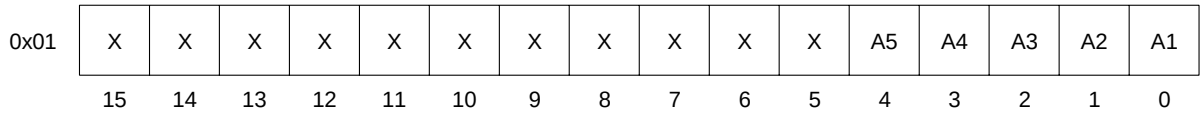

Figure 3.3 Bus Address Switch Register

3.3 Interrupt Select Register

This 16-bit read/write register at subaddress 0x0e selects the TUeDACS interrupt bit. TUeDACS interrupt bits 15..0 can be selected. Only bits 3..0 of this register are used.

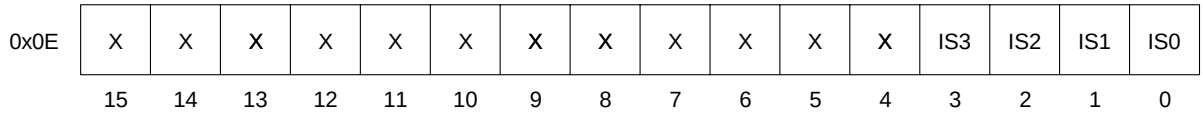

Figure 3.4 Interrupt Select Register

bit	mnemonic	R/W	description
15..4	-	-	not used, always reads as zero
3	IS3	R/W	Interrupt Select, bit 3
2	IS2	R/W	Interrupt Select, bit 2
1	IS1	R/W	Interrupt Select, bit 1
0	IS0	R/W	Interrupt Select, bit 0

IS3..IS0 (bits 3..0): Interrupt Select bits 3..0. Bit values 0x0000..0x000f in this register correspond with a TUeDACS interrupt bit selection of respectively 0..15.

3.4 Interface Identification Register

This 16-bit read-only register at subaddress 0x0f holds a value that uniquely determines the TUeDACS interface type. Bits 15..4 hold the identification code of the IEEE-488 interface. For the IEEE-488 interface, the identification code contained in bits 15..4 is 73 (decimal). The lower 4 bits of this register (bits 3..0) hold the revision code of the TUeDACS/3 IEEE-488 interface. Writing this register results in a bus error.

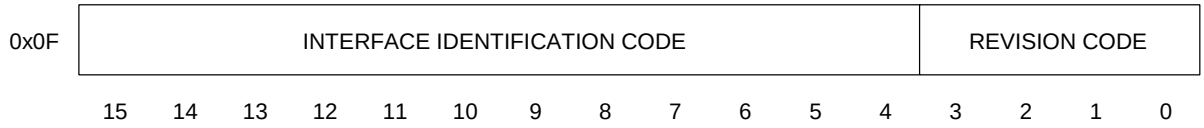

Figure 3.5 Interface Identification Register

3.5 Interrupt Status Register 0 / Interrupt Status Register 1

Events occuring on the IEEE-488 bus can be determined by reading read-only Interrupt Status Register 0 / Interrupt Status Register 1 at subaddresses 0x10 and 0x11, respectively. The bits in these registers are set when the appropriate events occur. The bits are cleared when reading corresponding Interrupt Status Register 0 / Interrupt Status Register 1.

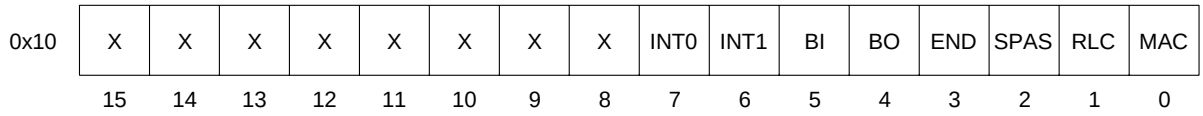

Figure 3.6 Interrupt Status Register 0

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	INT0	RO	INTerrupt occured in register 0
6	INT1	RO	INTerrupt occured in register 1
5	BI	RO	Data In Register is full. The BI bit is cleared when reading the Data In Register at subaddress 0x17
4	BO	RO	Data Out Register is empty. This bit is cleared when writing the Data Out Register at subaddress 0x17, and is set if the Data Out Register can accept new data
3	END	RO	EOI has occured with ATN false
2	SPAS	RO	the 9914 has requested service by setting the rsv bit of the Serial Poll Register (the 9914 is not a controller) and has been polled in serial poll.
1	RLC	RO	remote/local state change has occured.
0	MAC	RO	command received over the IEEE-488 bus which has resulted in the addressed state of the 9914 to change

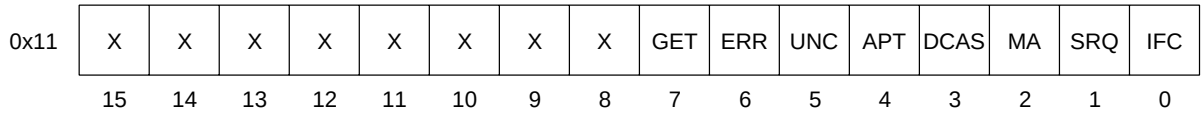

Figure 3.7 Interrupt Status Register 1

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	GET	RO	Group Execute Trigger command received over the IEEE-488 bus
6	ERR	RO	Incomplete source handshake error
5	UNC	RO	Unidentified command received
4	APT	RO	Secondary address received in extended addressing mode
3	DCAS	RO	SDC or DCL command received
2	MA	RO	Primary talk or listen address received (with ATN true)
1	SRQ	RO	Service Request has occured when the 9914 is controller
0	IFC	RO	IFC has occured

3.6 Interrupt Mask Register 0 and 1

When an event occurs on the IEEE-488 bus, the corresponding status bit of Interrupt Status Register 0 / Interrupt Status Register 1 at subaddresses 0x10 and 0x11, respectively, is set. If the corresponding bit of Interrupt Mask Register 0 / Interrupt Mask Register 1 is set, a TUeDACS interrupt is generated. The bits in the Interrupt Mask Registers 0/1 are identical to the bits in the Interrupt Status Registers 0/1 (see figures 3.5 and 3.6).

Before an event is able to interrupt the processor the respective mask bits must be set. Furthermore, the dai (disable all interrupts) auxiliary command must not be active.

Interrupt Mask Register 0 (see figure 3.6 for the bit assignment):

bit	mnemonic	R/W	description
15..6	-	-	not used, reads as zero
5	BI	WO	interrupt on byte input
4	BO	WO	interrupt on byte output
3	END	WO	interrupt on EOI with ATN false
2	SPAS	WO	interrupt on serial poll active state
1	RLC	WO	interrupt on remote/local change
0	MAC	WO	interrupt on addressed state change

Interrupt Mask Register 1 (see figure 3.7 for the bit assignment):

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	GET	RO	interrupt on Group Execute Trigger
6	ERR	RO	interrupt on incomplete source handshake
5	UNC	RO	interrupt on unidentified command
4	APT	RO	interrupt on address pass through. Setting this bit selects the address pass through feature of the 9914
3	DCAS	RO	interrupt on SDC command or DCL command
2	MA	RO	interrupt on my address
1	SRQ	RO	interrupt on service request (SRQ)
0	IFC	RO	interrupt on interface clear (IFC)

3.7 Address Status Register

The IEEE-488 bus address status of the interface can be determined by reading the read-only Address Status Register at subaddress 0x12.

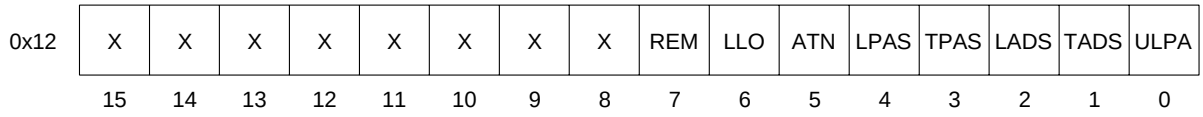

Figure 3.8 Address Status Register

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	REM	RO	Device in remote state
6	LLO	RO	Local lockout in operation
5	ATN	RO	ATN line active
4	LPAS	RO	9914 in listener primary addressed state
3	TPAS	RO	9914 in talker primary addressed state
2	LADS	RO	Device addressed to listen
1	TADS	RO	Device addressed to talk
0	ULPA	RO	Upper/Lower Primary Address bit

3.8 Auxiliary Command Register

This write-only register at subaddress 0x13 register is used to issue auxiliary commands. Two basic types of commands are implemented: pulsed and static. Use static commands to enable (set) or disable (clear) various features of the 9914. The pulsed commands stay active for one clock pulse after the Auxiliary command Register has been written.

A number of functions are of the Clear/Set (C/S) type. If a code is loaded with the C/S bit set, the function is selected and remains selected until the code is loaded with the C/S bit cleared. Other commands, such as Force EOI (feoi), have a pulsed mode of operation. These commands are always executed, regardless of the value of the C/S bit.

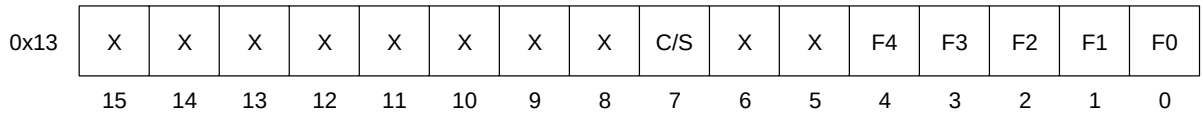

Figure 3.9 Auxiliary Command Register

bit	mnemonic	R/W	description
15..8	-	-	not used, always read as zero
7	C/S	WO	Clear or Set operation
6..5	-	-	not used, always read as zero
4	F4	WO	Function bit 4
3	F3	WO	Function bit 3
2	F2	WO	Function bit 2
1	F1	WO	Function bit 1
0	F0	WO	Function bit 0

An overview of the available auxiliary commands is given in table 3.1.

Hex code	Type	Mnemonic	Auxiliary Command
0x00	static	~swrst	Clear Software Reset
0x80	static	swrst	Set Software Reset
0x01	pulsed	nonvalid	Nonvalid Release DAC Holdoff
0x81	pulsed	valid	Valid Release DAC Holdoff
0x02	pulsed	rhdf	Release RFD Holdoff
0x03	static	~hdfa	Clear Holdoff On All Data
0x83	static	hdfa	Set Holdoff On All Data
0x04	static	~hdfe	Clear Holdoff On END Only
0x84	static	hdfe	Set Holdoff On END Only
0x05	pulsed	nbaf	New Byte Available False
0x06	static	~fget	Clear Force Group Execute Trigger
0x86	static	fget	Set Force Group Execute Trigger
0x07	static	~rtl	Clear Return To Local
0x87	static	rtl	Set Return To Local
0x08	pulsed	feoi	Send EOI With The Next Byte
0x09	static	~lon	Clear Listen Only
0x89	static	lon	Set Listen Only
0x0a	static	~ton	Clear Talk Only
0x8a	static	ton	Set Talk Only
0x0b	pulsed	gts	Go To Standby
0x0c	pulsed	tca	Take Control Asynchronously
0x0d	pulsed	tcs	Take Control Synchronously
0x0e	static	~rpp	Clear Request Parallel Poll
0x8e	static	rpp	Set Request Parallel Poll

0x0f	static	~sic	Clear Send Interface Clear
0x8f	static	sic	Set Send Interface Clear
0x10	static	~sre	Clear Send Remote Enable
0x90	static	sre	Set Send Remote Enable
0x11	pulsed	rqc	Request Control
0x12	pulsed	rlc	Release Control
0x13	static	~dai	Clear Disable All Interrupts
0x93	static	dai	Set Disable All Interrupts
0x14	pulsed	pts	Pass Through Next Secondary
0x15	static	~stdl	Clear Short T1 Delay
0x95	static	stdl	Set Short T1 Delay
0x16	static	~shdw	Clear Shadow Handshaking
0x96	static	shdw	Set Shadow Handshaking

Table 3.1 Auxiliary commands

3.8.1 Description of Auxiliary Commands

- Software Reset (swrst):

  writing this command causes the 9914 to enter a known idle state. In this idle state the IEEE-488 interface will not take part in any activity on the IEEE-488 bus. Table 3.2 shows the software reset conditions. The serial and parallel poll registers are not cleared. Both Interrupt Status Registers are cleared.

mnemonic	description
SIDS	Source idle state
AIDS	Acceptor idle state
TIDS	Talker idle state
TPAS	Talker primary idle state
LIDS	Listener idle state
LPAS	Listener primary state
NPRS	Negative poll response state
LOCS	Local state
CIDs	Controller idle state
SPIS	Serial Poll idle state
PPSS	Parallel Poll standby state
ADHS	DAC holdoff state
SHFS	Source holdoff state
ENIS	END idle state

Table 3.2 Software reset conditions

NOTE: after a hardware reset by setting the RST bit in the TUeDACS Status Word Register at subaddress 0x00, after issuing a software TUeDACS bus initilisation command or after a power-up, the swrst command is executed by the 9914. If this command is active, the 9914 can be set up in its initial state. The 9914 is held in the idle state until the ~swrst command is executed (i.e., the C/S bit is cleared). After the ~swrst command the 9914 becomes logically existent on the IEEE-488 bus.

- Release DAC holdoff (dacr or nonvalid)

  The Data Accepted holdoff allows time for the processor to respond to unrecognized commands, secondary addresses and Device Clear commands received over the IEEE-488 bus. The holdoff is released by the processor when the required action has been taken. This command is only useful when using the adress pass through feature of the 9914.

- Release RFD Holdoff (rhdf)

  Any Ready For Data holdoff caused by hdfa or hdfe is released.

- Holdoff on all data (hdfa)

  When the hdfa command is written to the Auxiliary Command Register a RFD holdoff will be caused on every data byte received over the IEEE-488 bus. The handshake must be completed after each byte has been received over the IEEE-488 bus using the rhfd auxiliary command. Normally the acceptor handshake is completed automatically by the 9914.

- Holdoff on End (hdfe)

  A RFD holdoff will occur when an end of data string message (EOI true with ATN false) is received over the IEEE-488 bus. The holdoff can be released using the rhdf auxiliary command.

- Set New Byte Available False (nbaf)

  If a talker is interrupted (ATN line goes true) the byte just stored in the data out register is sent as soon as the ATN line returns false. If, as a result of the interrupt, transmitting this byte is no longer required, its transmission may be suppressed by using the nbaf command.

- Force Group Execute Trigger (fget)

  This command cannot be used. The TR (TRigger) line of the 9914 is not connected.

- Return To Local (rtl)

  Provided the LLO has not been enabled, the remote/local bit is reset and an interrupt is generated (if enabled) in order to inform the processor it should respond to its front panel controls. The ~rtl command must be cleared before the device is able to return to remote control.

- Force EOI (feoi)

  This command causes the EOI line to go true when the next data byte is sent over the IEEE-488 bus. After sending this byte the EOI line is set false.

- Listen Only (lon)

  The listener state is activated until the ~lon command is sent or until deactivated by a bus command.

- Talk Only (ton)

  The talker state is activated until the ~ton command is sent or until deactivated by a bus command. The ton and lon commands are used when the 9914 is a controller. Using these commands, the 9914 is setup as a talker or listener. When the 9914 is a controller, sending the UNL command will not unlisten the 9914 and sending the UNT command will not untalk the 9914. When the lon command is active and the 9914 takes control (ATN line true) it becomes automatically a talker. After releasing control the 9914 is listener again.

- Go To Standby (gts)

  When the 9914 is the active controller sending this command will cause the ATN line to go false.

- Take Control Synchronously (tcs)

  Control is taken by the active controller and the ATN line is asserted. If the controller is not a listener, the shadow handshake feature must be used to monitor the handshake lines so the 9914 will synchronize with the talkers and listeners and only sets the ATN line true at the end of a byte transfer. This ensures no loss of data.

- Request Parallel Poll (rpp)

  This command is executed by the active controller to send the parallel poll command over the bus (the 9914 must be in controller active state). The status bits can be obtained by reading the Command Pass Through Register at subaddress 0x16. The poll is completed by sending the ~rpp command.

- Take Control Asynchronously (tca)

  This command is sent by the active controller to set the ATN line true and to gain control of the IEEE-488 bus. The command is executed immediately and data corruption or loss may occur.

- Send Interface Clear (sic)

  When the sic command is sent, the IFC line is set true. Only the system controller may execute this command. When executing this command the SYSC bit in the TUeDACS Status Word Register at subaddress 0x00 must be set. The controller is put in the CACS state (ATN line goes true). Sending the ~sic command will set the IFC line false.

- Send Remote Enable (sre)

  The sre command is sent by a system controller. The SYSC bit in the TUeDACS Status Word Register at subaddress 0x00 must be set in order to send this command. Writing the sre command will set the REN line true. Writing the ~sre command will set the REN line false.

- Request Control (rqc)

  When the 9914 is in the CIDS state this commands causes the 9914 to become the active controller. The ATN line is set true. When the TCT (Take Control) command has been recognized via the unidentified command pass through, this command must be sent by the processor. The 9914 waits for the ATN line to go false and then enters the CACS state.

- Release Control (rlc)

  The rlc command is used after a TCT command has been sent over the IEEE-488 bus. If the handshake is completed the ATN line is set false. Control is passed to another device.

- Disable All Interrupts (dai)

  All interrupts will be disabled, but the Interrupt Status Registers 0/1 at suabdresses 0x10 and 0x11 are not affected.

- Pass Through Next Secondary (pts)

  This feature is used to carry out a remote configuration of parallel poll. The parallel poll configure (PPC) command is passed through the 9914 as an unrecognized command and is identified by the processor. The pts command is loaded and the next byte received by the 9914 is passed through via the Command Pass Through Register at subaddress 0x16. This would be the parallel poll enable (PPE), which is read by the processor.

- Set T1 Delay (sdt1)

  The sdt1 command sets the T1 delay to 6 clock cycles (1.2 µs). The ~sdt1 command sets the T1 delay to 11 clock cycles (2.2 µs).

- Shadow handshake (shdw)

  This feature enables the controller to carry out the listener handshake without participating in a data transfer. The NDAC line is set false a maximum of 3 clock cycles after DAV is received and NRFD is allowed to go false as soon as DAV is removed. The shadow handshake function allows the tcs command to be synchronized with the Acceptor Not Ready State (ANRS) so that ATN can be re-asserted without causing loss or corruption of data

3.9 Address Register

The IEEE-488 bus address of the IEEE-488 interface must be stored in this write-only register at subaddress 0x14.

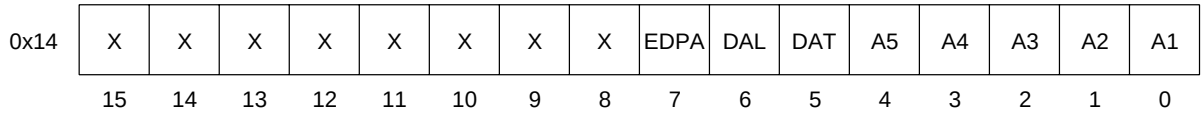

Figure 3.10 Address Register

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	EDPA	WO	Enable dual primary addressing.
6	DAL	WO	Disable listen functions.
5	DAT	WO	Disable talker functions.
4	A5	WO	Device primary address, bit 5
3	A4	WO	Device primary address, bit 4
2	A3	WO	Device primary address, bit 3
1	A2	WO	Device primary address, bit 2
0	A1	WO	Device primary address, bit 1

Bits 4..0 (A5..A1) of this register contain the primary address of the device. After a power-up, reset or a swrst auxiliary command with the C/S bit set (see section 3.8.1), the address may be loaded. The address must be loaded by copying the first 5 bits of the Bus Address Switch Register at subaddress 0x01 (B4..B0) into the first 5 bits (A5..A1) of the 9914 Address Register.

3.10 Bus Status Register

The processor may obtain the status of all IEEE-488 bus management and handshake lines by reading the read-only Bus Status Register at subaddress 0x13. The bus signals are not stored. The information obtained from the 9914 are the signal states at time of reading.

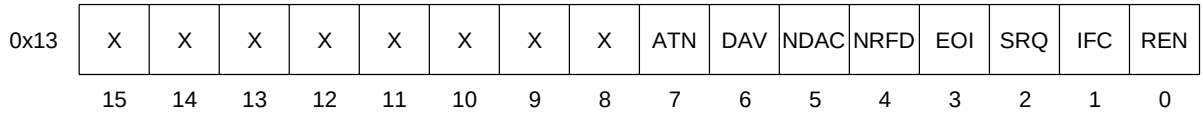

Figure 3.11 Bus Status Register

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	ATN	RO	Attention
6	DAV	RO	Data Valid
5	NDAC	RO	Not Data Accepted
4	NRFD	RO	Not Ready For Data
3	EOI	RO	End-Or-Identify
2	SRQ	RO	Service Request
1	IFC	RO	Interface Clear
0	REN	RO	Remote Enable

3.11 Serial Poll Register

This write-only register at subaddress 0x15 contains the byte transmitted when the active controller (not the 9914) carries out a serial poll on the device. This register is cleared by a hardware reset, or by setting the RST bit in the TUeDACS Status Word Register at subaddress 0x00. The Serial Poll Register is *not* cleared by a software reset.

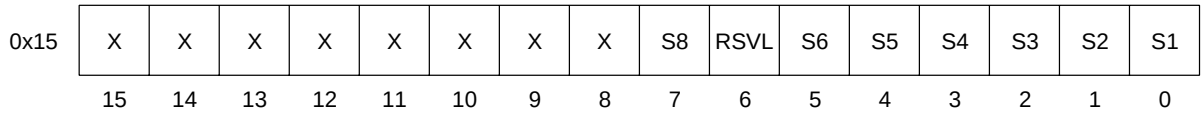

Figure 3.12 Serial Poll Register

bit	mnemonic	R/W	description
15..8	-	-	not used, reads as zero
7	S8	WO	Serial Poll bit 8
6	RSV	WO	Request Service
5	S6	WO	Serial Poll bit 6
4	S5	WO	Serial Poll bit 5
3	S4	WO	Serial Poll bit 4
2	S3	WO	Serial Poll bit 3
1	S2	WO	Serial Poll bit 2
0	S1	WO	Serial Poll bit 1

Bits S8 and S6 to S1 contain device dependent information while bit 6 contains the request service bit (RSV). When this bit is set, the SRQ line becomes true. When the active controller responds (not the 9914) by carrying out a serial poll on the device, the SRQ line returns to the passive false state automatically. The RSV bit must be cleared by the processor after the service has been carried out. A new service request cannot be generated until the RSV bit has been cleared.

3.12 Command Pass Through Register

This read-only register at subaddress 0x16 can be used to inspect the IEEE-488 DIO lines directly. It has no storage and should only be used when the DIO lines are known to be in a steady state. It is used by an active controller to read the results of a parallel poll.

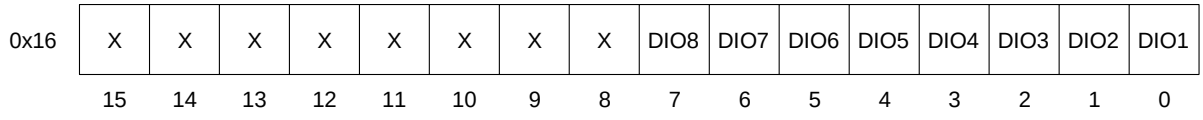

Figure 3.13 Command Pass Through Register

3.13 Parallel Poll Register

The contents of this write-only register at subaddress 0x16 are output when a parallel poll is conducted by an active controller. It must be loaded by the processor before the poll takes places (usually during intialisation when swrst is active). This register is cleared by a hardware reset, but *not* by a swrst command.

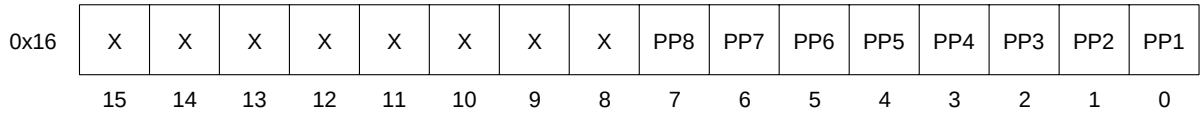

Figure 3.14 Parallel Poll Register

3.14 Data In Register

When addressed as a listener, this read-only register at subaddress 0x17 holds the data from the IEEE-488 bus. The BI bit (Byte In) in Interrupt Mask Register 0 at subaddress 0x10 is set and the NRFD line is held true until the processor has read the Data In Register. Unless a holdoff has been selected (hdfa or hdfe) the acceptor handshake is completed automatically. In the case of a ready for data holdoff, the handshake must be completed by the processor using a rhdf auxiliary command. The write-only Data Out Register at subaddress 0x17 is not affected by reading the Data In Register.

0x17	X	X	X	X	X	X	X	X	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 3.15 Data In Register

3.15 Data Out Register

When acting as talker or controller the write-only Data Out Register at subaddress 0x17 is used to transfer data bytes or commands from the processor to the IEEE-488 bus.

0x17	X	X	X	X	X	X	X	X	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 3.16 Data Out Register

If the 9914 has previously been placed in the controller active state, commands are sent with the ATN line active true. In the talker active state (device dependent data is sent) ATN is held false. In both cases the source handshake function is automatically performed by the 9914.

When the byte has been sent over the IEEE-488 bus, the BO bit in Interrupt Mask Register 0 at subaddress 0x10 is set and a new byte may be loaded by the processor. In order to prompt the loading of the first byte, the BO bit is set when the 9914 enters the talker mode.

In some circumstances the ATN line may be set true by the active controller (not the 9914) after a byte has been loaded into the Data Out Register but before it is sent over the bus. This byte will be sent immediately after the ATN line goes false unless the nbaf command is given.

The read-only Data In Register at subaddress 0x17 is not affected by writing into the Data Out Register.

4. DIP switch settings

The IEEE-488 bus address can be set using an 8-position DIP switch of which switch positions 1..5 are used. The IEEE-488 bus address can be selected by setting the 5 bit DIP switch to the desired address. A switch in the ‘ON’ position represents a logical 1, a switch in the ‘OFF’ position represents a logical 0. The switch labeled A1 represents the Least Significant Bit (LSB) of the address, the switch labeled A5 represents the Most Significant Bit (MSB). A value in the range of 0..31 can be selected.

5. LED indicators

The following LED indicators are located on the front panel of the IEEE-488 interface:

TE	Talker Enable. This LED illuminates if the IEEE-488 interface is a talker on the IEEE bus.
SYSC	SYStem Controller. This LED illuminates if the IEEE-488 interface is a controller on the IEEE bus
RSRQ	Remote Service ReQuest. This LED illuminates if the IEEE-488 interface receives a service request from a device on the IEEE bus
MSRQ	My Service ReQuest. This LED illuminates if the IEEE-488 interface generates a service request